

NEWS RELEASE

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Verific Adds Support for PSL/Sugar to its HDL Component Software *Move Designed to Enable Assertion-Based Verification*

Alameda, Calif. — February 9, 2004 — Verific Design Automation, the leading provider of Verilog and VHDL front ends for electronic design automation (EDA) applications, today said that its products now support Accellera's property specification language (PSL)/Sugar. This means that all of its hardware design language (HDL) component software packages now include a PSL/Sugar reader, and will enable assertion-based verification.

“The PSL/Sugar Consortium is pleased that Verific is offering assertion-based specifications within its HDL component software packages,” says Harry Foster, the consortium's formal verification technical committee chair. “This allows EDA companies to swiftly introduce native PSL/Sugar support in their verification tools. We were waiting for something like this to happen.”

Additionally, Verific has joined the PSL/Sugar Consortium, an organization intent on helping hardware designers adopt and implement PSL/Sugar and its methodologies to

speed system-level design and verification. PSL/Sugar, based on the IBM Sugar assertion language, is a powerful, concise language for assertion specification and complex modeling. It provides an interoperable specification language to exchange hardware specifications and develop seamless tool integration.

“PSL/Sugar is helping meet the demands of complex chip design,” says Rob Dekker, president of Verific. “We believe in supporting standards and PSL/Sugar is a comprehensive standard which will fully enable assertion-based verification for Verilog, VHDL and mixed-language designs. That’s why we’ve added it to our growing list of products and joined the PSL/Sugar Consortium.”

Pricing and Availability of HDL Component Software Package

The latest versions of Verific’s component software packages are available now, all written in platform-independent C++ that compiles on Solaris, HP-UX, Linux and Windows platforms. In addition to the PSL/Sugar reader, products include VHDL and Verilog readers and register transfer level (RTL) databases. Verific’s PSL parsers support both Verilog- and VHDL-style PSL, and parses PSL either in-line with the HDL or from a separate specification file. All come with online support and maintenance. Pricing starts at \$25,000 for the PSL package per language.

For more details, contact Rick Carlson, Verific’s vice president of sales. He can be reached at (970) 946-1755 or via email at rick@verific.com. Or, visit Verific’s website located at: <http://www.verific.com>.

Information on PSL/Sugar can be found at the PSL/Sugar Consortium website found at: <http://www.pslsugar.org>.

About Verific Design Automation

Verific Design Automation was founded in 1998 by electronic design automation (EDA) industry veteran Rob Dekker. It develops and sells C++ source code-based Verilog and VHDL front ends — parsers, analyzers and elaborators — as well as a generic hierarchical netlist database for EDA applications. Verific's technology has been licensed in many applications, combined shipping more than 20,000 end-user copies. Corporate headquarters is located at: 1516 Oak Street, Suite 115, Alameda, Calif. 94501. Telephone: (510) 522-1555. Facsimile number: (510) 522-1553. Email: info@verific.com. Website: <http://www.verific.com>.

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