

# ***NEWS RELEASE***

## **Verific Becomes Stelar's HDL Technology Partner** *Verific HDL Component Software Integrated With Stelar's Graphical and Textual Design Environment*

**Portland, Ore., and Alameda, Calif. — November 9, 2004** — Stelar Tools, Inc., a Portland, Ore.-based electronic design automation (EDA) startup, today said it has integrated Verific Design Automation's hardware description language (HDL) Component Software with its graphical and textual design environment.

Verific's HDL Component Software — C++ source code-based Verilog and VHDL parsers, analyzers and elaborators — acts as the front end to Stelar's toolset for creating, exploring, navigating, analyzing, documenting and modifying a design within an existing design environment.

According to Scott Bloom, Stelar's vice president of engineering, Verific offered Stelar a cost-effective means of getting the quality VHDL and Verilog parser it needed in the time it needed it. He noted that all of Stelar's 100 benchmark designs could be read and elaborated by the Verific parser without modification.

Bloom says, "The runtime and memory footprint is on par or vastly superior to all other parsers that we evaluated. Support has been superb, as well. No issue took longer than three days to have a workaround, and all enhancement requests were granted."

Adds Joe Tanous, Stelar's chief executive officer: "Verific was willing to work with us pre-funding and went out of its way to help us build a quick prototype to show to investors."

"We strive to offer each of our customers the kind of support that Stelar has experienced," says Michiel Ligthart, Verific's vice president of operations. "Stelar is an

emerging EDA company with loads of promise. Our intention is to be part of its success every step of the way.”

### **About Stellar Tools, Inc.**

Founded in 2003, Stellar Tools, Inc. is a privately held company that delivers the first true smart graphical and intelligent textual design creation and analysis environment for large, complex HDL designs. This enables designers and verification engineers to rapidly reach RTL Closure by offering them the ability to explore, navigate, analyze, document, and create a design using their current design methodology and tools. RTL Closure is the process of getting the design clean at the register transfer level, before synthesis, to shorten development time and reduce development cost. Further information about Stellar can be found at [www.stelartools.com](http://www.stelartools.com).

### **About Verific Design Automation**

Verific Design Automation was founded in 1998 by electronic design automation (EDA) industry veteran Rob Dekker. It develops and sells C++ source code-based Verilog and VHDL front ends — parsers, analyzers and elaborators — as well as a generic hierarchical netlist database for EDA applications. Verific’s technology has been licensed in many applications, combined shipping more than 20,000 end-user copies. Corporate headquarters is located at: 1516 Oak Street, Suite 115, Alameda, Calif. 94501. Telephone: (510) 522-1555. Facsimile number: (510) 522-1553. Email: [info@verific.com](mailto:info@verific.com). Website: <http://www.verific.com>.

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