

NEWS RELEASE

For more information, contact:

Nanette Collins
Public Relations for Verific
(617) 437-1822
nanette@nvc.com

Verific Design Automation Adds Jasper Design Automation to Customer List *Formal Verification Supplier Selects Verific HDL Component Software for JasperGold*

Alameda, Calif. — May 24, 2005 — Verific Design Automation today announced that Jasper Design Automation, provider of breakthrough high-level formal verification solutions, has selected Verific's Hardware Description Language (HDL) Component Software as the SystemVerilog, Verilog and VHDL language parser for its JasperGold™ formal verification solution.

“Verific made choosing its HDL Component Software easy for us,” notes Nafees Qureshy, vice president of engineering at Jasper Design Automation. “Verific has a reputation for product quality, reliability and customer support. The software saved us at least six months of development time. In this demanding economic environment, that’s an important advantage.”

The HDL Component Software Package

“We are adding value to EDA suppliers who need to focus on their core competencies,” said Verific’s President Rob Dekker. “Jasper is free to focus on its core

competency — high-level formal verification — because our core competency is the HDL front end, and we welcome the opportunity to support Jasper.”

Verific offers a number of component software packages, all written in platform-independent C++ that compiles on Solaris, HP-UX, Linux and Windows platforms. Products include VHDL and Verilog parsers, analyzers, and elaborators, as well as an RTL database. All products are licensed as source code and come with online support and maintenance.

For more details, contact Rick Carlson, Verific’s vice president of sales. He can be reached at (970) 946-1755 or via email at rick@verific.com. Or, visit Verific’s website located at: <http://www.verific.com>.

About Verific Design Automation

Verific Design Automation was founded in 1999 by electronic design automation (EDA) industry veteran Rob Dekker. It develops and sells C++ source code-based SystemVerilog, Verilog and VHDL front ends — parsers, analyzers and elaborators — as well as a generic hierarchical netlist database for EDA applications. Verific’s technology has been licensed in many applications, combined shipping more than 45,000 end-user copies. Corporate headquarters is located at: 1516 Oak Street, Suite 115, Alameda, Calif. 94501. Telephone: (510) 522-1555. Facsimile number: (510) 522-1553. Email: info@verific.com. Website: <http://www.verific.com>.

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