

NEWS RELEASE

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Safelogic Adds Verific's HDL Component Software to Latest Release of Verifier *Verilog, VHDL Front End Integrated with Formal Verification Tool,*

Alameda, Calif. — April 5, 2004 — Electronic Design Automation (EDA)

supplier Verific Design Automation today announced that Safelogic has integrated its Hardware Description Language (HDL) Component Software as the Verilog and VHDL front end of Verifier®, a formal verification property checker.

“Verific’s HDL Component Software is the industry standard in quality and ease of use,” says Krister Nilsson, Safelogic’s CEO. “We are excited about the latest version of Verifier, in large measure due to the addition of a Verilog and VHDL front end, and hope that our customers will think the same.”

The HDL Component Software Package

“Safelogic is a company with growing momentum,” adds Rob Dekker, Verific’s president. “It gives us great pleasure to work with its team.”

Verific offers a number of component software packages, all written in platform-independent C++ that compiles on Solaris, HP-UX, Linux and Windows platforms.

Products include VHDL and Verilog parsers, analyzers, and elaborators, as well as a register transfer level (RTL) database. All products are licensed as source code and come with online support and maintenance.

For more details on Verific's HDL Component Software, contact Rick Carlson, its vice president of sales. He can be reached at (970) 946-1755 or via email at rick@verific.com. Or, visit Verific's website located at: <http://www.verific.com>.

About Safelogic

Safelogic is an EDA company developing groundbreaking tools for improved simulation, formal analysis and verification of RTL designs. Products include Safelogic Monitor® — plug-in for property simulation, Safelogic Verifier® — formal property checker, and Safelogic ASG® - automatic stimuli generator. For more information, visit www.safelogic.se.

About Verific Design Automation

Verific Design Automation was founded in 1998 by electronic design automation (EDA) industry veteran Rob Dekker. It develops and sells C++ source code-based Verilog and VHDL front ends — parsers, analyzers and elaborators — as well as a generic hierarchical netlist database for EDA applications. Verific's technology has been licensed in many applications, combined shipping more than 20,000 end-user copies. Corporate headquarters is located at: 1516 Oak Street, Suite 115, Alameda, Calif. 94501. Telephone: (510) 522-1555. Facsimile number: (510) 522-1553. Email: info@verific.com. Website: <http://www.verific.com>.

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