

## ***NEWS RELEASE***

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### **Silicon Navigator Licenses Verific's HDL Component Software** *Verific HDL Component Software Integrated With Silicon Navigator's OpenAccess Framework*

**Alameda, Calif. — March 2, 2005** — Verific Design Automation today said that Silicon Navigator Corporation, also known as SiNavigator(TM), has licensed its hardware description language (HDL) Component Software.

Verific's HDL Component Software — C++ source code-based SystemVerilog, Verilog and VHDL parsers, analyzers and elaborators — are integrated with Silicon Navigator's OpenAccess technology that enables integrated circuit (IC) timing, placement, and optimization. Silicon Navigator is leveraging the OpenAccess database created by Cadence Design Systems Inc. (NYSE: CDN) and available in Open Source from the Silicon Integration Initiative (Si2).

J. George Janac, founder and chief executive officer (CEO) of Silicon Navigator, says: "We have done extensive evaluation of Verilog and VHDL software. Verific's Verilog and VHDL processing has consistently outperformed the competition. We see it as a key component to our Open Access based strategy. Verific has business models which are directly in line with the growing field of EDA software component licensing, which makes it an excellent partner. We have developed a cooperative and synergistic relationship."

“Silicon Navigator is breaking new ground with its OpenAccess-based framework and engines,” adds Michiel Ligthart, Verific’s chief operating officer. “We’re pleased to be helping change the EDA landscape by having our HDL Component Software part of its product line.”

### **About Silicon Navigator**

Founded in late 2003, Silicon Navigator Corporation (or SiNavigator) is a private Electronic Design Automation (EDA) software company whose products represent the next generation of Library Smart™ tools for chip design.

Silicon Navigator corporate headquarters are located at: 10050 North Wolfe Road, Suite SW2-260, Cupertino, Calif. 95014. Telephone: 408-200-0280. Facsimile: 408-200-0281. Email: [info@sinavigator.com](mailto:info@sinavigator.com). Website: <http://www.sinavigator.com>.

### **About Verific Design Automation**

Verific Design Automation was founded in 1999 by electronic design automation (EDA) industry veteran Rob Dekker. It develops and sells C++ source code-based SystemVerilog, Verilog and VHDL front ends — parsers, analyzers and elaborators — as well as a generic hierarchical netlist database for EDA applications. Verific’s technology has been licensed in many applications, combined shipping more than 30,000 end-user copies. Corporate headquarters is located at: 1516 Oak Street, Suite 115, Alameda, Calif. 94501. Telephone: (510) 522-1555. Facsimile number: (510) 522-1553. Email: [info@verific.com](mailto:info@verific.com). Website: <http://www.verific.com>.

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