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Forte Renews License for Verific Design Automation Software

Verific's Verilog HDL Software Integrated with Forte's CellMath Designer Datapath Synthesis

ALAMEDA, CALIF. — April 22, 2010 — Verific Design Automation, supplier of de facto standard front-end software to the EDA and semiconductor community, announced today that Forte Design Systems has renewed its license for Verific's HDL software for use with its CellMath Designer(tm) datapath synthesis.

The license was originally issued in 2006 to Arithmatica Ltd., a company acquired by Forte last year. At that time, Verific's Verilog parser and register transfer level (RTL) elaborator were integrated with CellMath Designer to provide tighter integration flow for Verilog users and easy-to-use syntax to specify datapath structures.

"We're delighted to be working with Forte as it enhances CellMath Designer's value to the engineering community," says Michiel Ligthart, Verific's chief operating officer. "Forte is extending its powerful brand into a new market segment through product excellence and quality of results."

Project teams use CellMath Designer as an optimization step prior to logic synthesis to reduce area, improve performance and lower power consumption for datapath-intensive design blocks. Using CellMath intellectual property (IP), CellMath Designer combines advanced synthesis techniques with datapath architectures to reduce circuit area and power and for circuit speeds unachievable through other means. CellMath Designer works in conjunction with general logic synthesis products and utilizes existing RTL code, synthesis scripts and technology libraries to allow designers to quickly improve results.

Concludes Sean Dart, Forte's president and chief executive officer: "Verific's reputation for solid product offerings and strong customer support are well earned. We've been impressed with Verific's willingness to work with us through the transition and its commitment to making CellMath Designer a 'must-have' datapath synthesis tool."

About Verific Design Automation

Verific Design Automation, with offices in Alameda, Calif., and Kolkata, India, provides de facto standard SystemVerilog, Verilog and VHDL front-end software founded in 1999 by EDA industry veteran Rob Dekker. Verific's software is used worldwide by the EDA and semiconductor community in synthesis, simulation, formal verification, emulation, debugging, virtual prototyping, and design-for-test applications, which combined have shipped more than 40,000 copies. Corporate headquarters is located at: 1516 Oak Street, Suite 115, Alameda, Calif. 94501. Telephone: (510) 522- 1555. Facsimile number: (510) 522-1553. Email: info@verific.com. Website: www.verific.com.

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