

Verific's Parser Platform

- SystemVerilog IEEE 1800-2005/2009 parser, analyzer, and elaborators
- VHDL IEEE 1076-1993 parser, analyzer, and elaborators
- Verilog IEEE 1364-1995/2001/2005 pre-processor, parser, analyzer, and elaborators
- Full mixed SystemVerilog / VHDL language support
- Verilog-AMS 2.3 parser and analyzer
- PSL IEEE 1850 parser and analyzer for VHDL and Verilog
- SDF 2.1 parser
- Hierarchical, technology independent database
- Verilog 2001, SystemVerilog test suites

"It would have been very difficult to achieve our language coverage and quality goals in ISE without the help of the Verific parsers and elaborators. Verific has become the industry standard for good reason."

Dan Gibbons, senior director for Interactive Design Tools, Xilinx

"Quartz Formal, our state-of-the-art equivalence checker, required a language front end that would match its quality and performance. We found all that and more in Verific's Verilog, VHDL, and SystemVerilog parsers / elaborators. Their software is great and matched with excellent support."

Rajeev Madhavan, chairman & CEO, Magma Design Automation

Verific Design Automation builds SystemVerilog and VHDL Parser Platforms which enable its customers to develop advanced EDA products quickly and at low cost.

Verific's Parser Platform is distributed as C++ source code and compiles on all 32 and 64 bit Unix, Linux, and Windows operating systems.

Verific's Parser Platform is in production and development use today at numerous companies worldwide, from EDA start-ups to established Fortune 500 semiconductor vendors. Applications vary from formal verification to synthesis, simulation, emulation, virtual prototyping, in-circuit debug, and design-for-test.

Benefits of Verific's Parser Platform

Time to Market

- At least 9 month head start with production proven RTL technology
- No need to recruit and staff your own HDL software team
- No need for extensive test and debug of your HDL solution

Focus

- Concentrate on the strategic, differentiated core of your application
- Don't waste time and talent on non-strategic HDL software

Quality

- Prevent lost sales due to immature HDL front-end
- Prevent high support costs due to bugfix releases and workarounds

License Models

- Our licenses are always royalty-free. We ship Source Code to our customers, allowing you full control over modifications, extensions, integration, and compilation
- Our time-based licenses have no upfront cost, can be cancelled anytime, and include maintenance and support
- If there is a technical match, we will find a license arrangement that fits your needs

Verific's software is integrated in a variety of EDA products, including:

Actel	Libero
Altera	Quartus II
Altium	Nexar
Apache	PowerTheater, -Artist
Axiom	@Verifier
CLKDA	Amber
Calypto	SLEC, PowerPro
Concept Eng.	RTLVision Pro
DAFCA	ClearBlue
DeFacTo	HiDFT-Scan
EVE	ZeBu
Forte	CellMath Designer
GateRocket	RocketDrive
HDL Works	HDL Companion
iRoC	SoCFIT
Jasper	JasperGold
Lattice Semi	ispLever
Magma	FineSim
Magma	QuartzFormal
NEC	CyberWorkBench
NXP	RTL DfT
Oasys	RealTime Designer
Real Intent	Ascent, Meridian
Real Intent	PureTime
Rocketick	RocketSim
S2C	Tai IP
Springsoft	Certitude
Synopsys	MVSIM
Tiempo	ACC
Vennsa	onPoint
Xilinx	ISIM, IST

“Without Verific, our internal SystemVerilog development effort would have been a long, difficult process. Verific's language solutions, combined with Jasper's leading assertion synthesis technology, have contributed to our leading position in formal verification for standard assertion and design languages.”

Claudionor Coelho, vice president of engineering, Jasper

“The decision to work with Verific was an easy one for us because its HDL Component Software is the standard front-end source code. Verific's team is exceptional and its support is unmatched. Our experience working with Verific has been excellent.”

Gagan Hasteer, vice president of engineering, Calypto

Verific is a Platform

“Platforms help users create products, businesses, communities, and networks of their own. If it is open and collaborative, those users may in turn add value to the platforms.”

Jeff Jarvis

What Would Google Do

Production Proven SystemVerilog and VHDL Platforms

More than 50 EDA, FPGA and semiconductor companies are shipping products incorporating Verific's SystemVerilog and VHDL front-ends, with a combined customer base of more than 40,000 users. The principal developer of Verific's Parser Platform wrote VHDL and Verilog parsers, analyzers, and elaborators for two different synthesis products at a major EDA company prior to architecting the Verific solution. Instead of writing your own, you can buy and incorporate our C++ source code, fully tested and production proven. And, because Verific ships Source Code, you still retain full control over all modifications, extensions and integration.

Royalty-free, Time-based Source Code Licenses

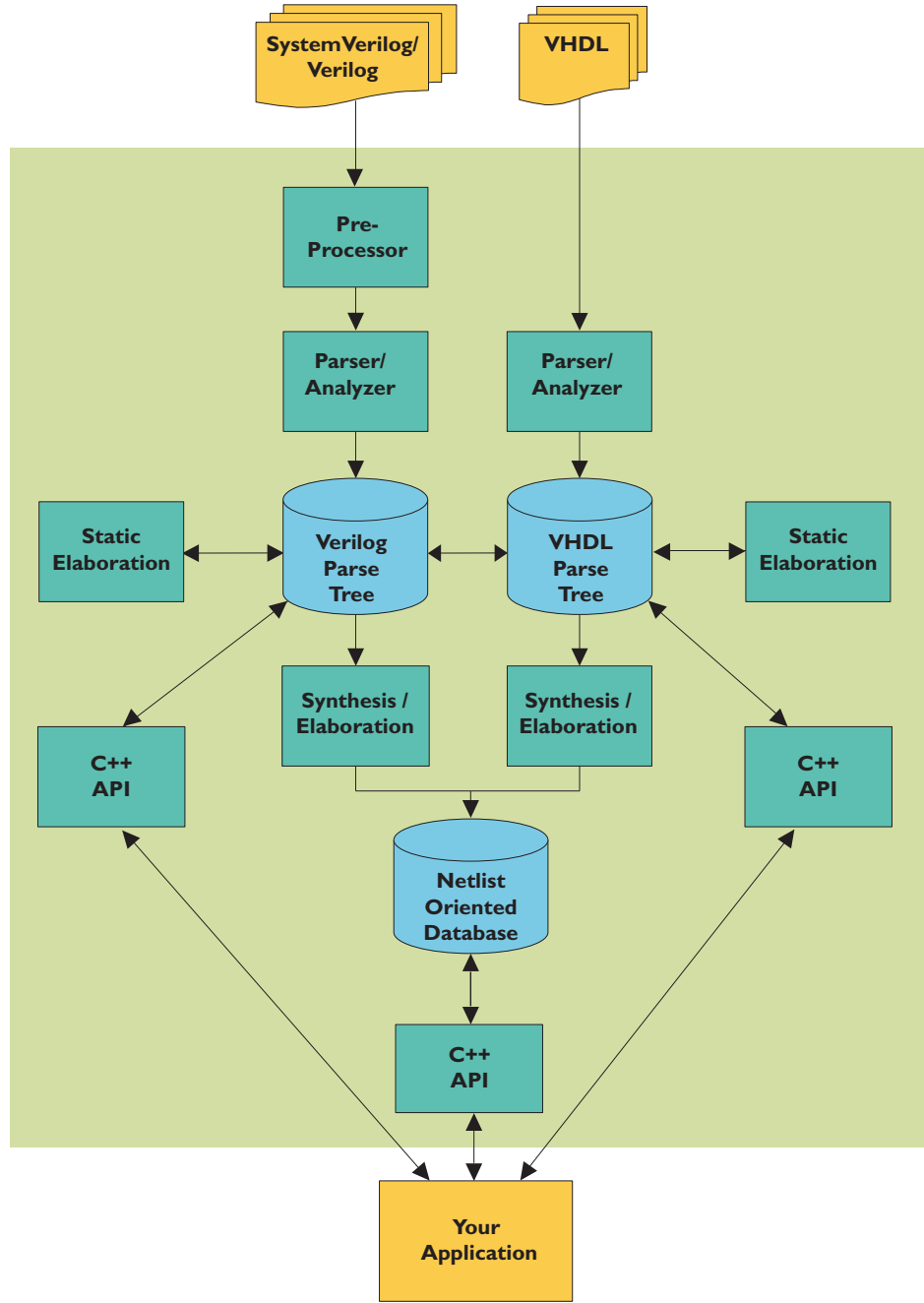
Verific Design Automation ships its software as C++ source code, including makefiles for Unix and Windows platforms. Our time-based licenses are royalty-free and include maintenance and support.

“Verific's HDL Component Software has become the industry standard and for good reason. The software is first rate and the support is outstanding. Verific is an excellent development partner.”

Luc Burgun, CEO and president, EVE

Verific
Design Automation®

Verific's
Parser
Platform



"The speed of the Verific software is very impressive. We are seeing 10x throughput increases over the previous solution we used to manage mixed Verilog and VHDL designs."

Tom Miller, vice president
of engineering, Apache

"Quartus II, Altera's flagship design software includes integrated VHDL and Verilog HDL technology from Verific. Verific's software meets the high standard of quality our customers have come to expect from us."

Misha Burich, Senior VP
Software Engineering, Altera



VHDL Platform

- Parses, analyses and elaborates 15,000 lines/second RTL, 30,000 lines/second flat-netlist code. (Average throughput, 2 Ghz Xeon, Red Hat Linux 8.0.)
- 100% VHDL 93 (IEEE 1076-93) as well as VHDL 87 (IEEE 1076) language coverage.
- Includes synthesis subset checking.
- Wide language subset support for elaboration, including IEEE 1164, multiple libraries, records, multi-dimensional arrays, generics, configurations, user-defined and overloaded functions/procedures/types, variable-indexing etc..
- Support for all standard and de-facto standard synthesis packages.
- Support for all Cadence, Mentor Graphics, and Synopsys synthesis pragmas.
- Downstream error handling support with line/file origination storage in RTL database.
- Application specific compile and run-time switches (don't care info, object preservation, etc.)

SystemVerilog / Verilog Platform

- Parses, analyses and elaborates 20,000 lines/second RTL, 50,000 lines/second flat-netlist code. (Average throughput, 2 Ghz Xeon, Red Hat Linux 8.0).
- 100% SystemVerilog IEEE 1800-2005/2009, including Verilog IEEE 1364-1995 / 2001 language coverage.
- Includes synthesis subset checking.
- Built-in Verilog pre-processor.
Wide language subset support for elaboration, including memory, named ports, tasks, functions,
- variable-indexing, string constants, UDP tables, etc..
- Verilog XL compliance with unknown module instantiation, and -y/-v file search mechanisms.
- Support for all Cadence, Mentor Graphics, and Synopsys synthesis pragmas.
- Downstream error handling support with line/file origination storage in RTL database.
Application specific compile and run-time switches (don't care info, object preservation, etc.).

RTL Database

- Average memory usage approximately 300 bytes / instance.
- Full hierarchy support, with grouping/ungrouping, etc..
- Full support for any number of libraries, and no restrictions on library interaction (instantiations across different libraries).
- Support for buses.
- Compact storage of line, file and column origination info from RTL parsers.
- Simple and clean data model with procedural interface for easy integration with your existing database.

Support and Maintenance

- On-line, customer accessible defect and enhancement tracking.
- Standard monthly releases with enhancements and improvements.
- 24 hour turnaround for critical defects.

About Verific Design Automation

Verific Design Automation, with offices in Kolkata, India, and Alameda, CA, was founded in 1999 by EDA industry veteran Rob Dekker. Prior to founding Verific, Dekker was a software developer, manager, and director at Exemplar Logic. The defacto standard for SystemVerilog and VHDL front-ends, Verific's software is used worldwide in synthesis, formal verification, emulation, debugging, virtual prototyping, and design-for-test applications, which combined have shipped over 40,000 copies.



May 2010

