



head and shoulders above the rest...



Verific Software Serves as Front End to Oasys Design Systems RealTime Designer

VHDL Analyzer Software Supplied by Verific to Provide Reliable Front End

ALAMEDA, CALIF. — November 17, 2009 — Oasys Design Systems announced today that RealTime Designer(TM), Chip Synthesis(TM) software capable of synthesizing register transfer level (RTL) code for 100-million gate designs, now includes support for VHDL through de facto standard front-end software from Verific Design Automation.

Verific licensed its VHDL analyzer to Oasys, giving RealTime Designer a common, proven and reliable front end for its unique Physical RTL synthesis. RealTime Designer is in production flows at leading-edge semiconductor and systems companies worldwide.

Verific's software serves as the front end to numerous Field Programmable Gate Array (FPGA) and Electronic Design Automation (EDA) tools for synthesis, simulation and verification applications. The software is written in platform-independent C++ that compiles on Solaris, HP-UX, Linux and Windows platforms. Each is licensed as source code and come with support and maintenance.

"Integrating Verific's software with RealTime Designer had been a part of our product planning and development from the beginning because of its superior quality," notes Paul van Besouw, president and chief executive officer of Oasys. "Verific's customer support group has a reputation for outstanding service and each member lived up to that reputation."

"Oasys' RealTime Designer has the potential to be a game-changing EDA tool," says Michiel Ligthart, Verific's chief operating officer. "Anytime one can reduce logic synthesis and optimization runtime by a factor of 10 it will get noticed by the user community."

About Verific Design Automation

Verific Design Automation, with offices in Alameda, Calif., and Kolkata, India, is a leading provider of SystemVerilog, Verilog and VHDL front-end software founded in 1999 by EDA industry veteran Rob Dekker. Verific's software is used worldwide in synthesis, simulation, formal verification, emulation, debugging, virtual prototyping, and design-for-test applications, which combined have shipped more than 40,000 copies. Corporate headquarters is located at: 1516 Oak Street, Suite 115, Alameda, Calif. 94501. Telephone: (510) 522-1555. Facsimile number: (510) 522-1553. Email: Email Contact. Website: www.verific.com.

Verific Design Automation acknowledges trademarks or registered trademarks of other organizations for their respective products and services.

