



head and shoulders above the rest...



Real Intent, Verific Celebrate Eight-Year Collaborative Partnership

Since 2001, Real Intent has Licensed Verific's SystemVerilog, VHDL Software

Alameda, Calif. — April 7, 2009 — Real Intent Inc., the leading supplier of formal verification software for electronic design, and Verific Design Automation each celebrates its 10 year anniversary in 2009 and a long-term partnership that spans the last eight years.

Since 2001, Verific, the leading provider of SystemVerilog, Verilog and VHDL front-end software, has supplied Real Intent with a VHDL parser and analyzer. This thriving relationship was extended in 2007 when Verific's SystemVerilog parser was integrated with Real Intent's internally developed elaborator.

"Real Intent congratulates Verific on its 10th anniversary and knows first hand why Verific has had long-term success," says Carol Hallett, vice president of World Wide Sales and Marketing. "We have had a winning collaboration with Verific over a long period of time and knew where to go when we needed to upgrade to SystemVerilog."

"Real Intent has passed the 10-year mark with breakthrough formal verification software," adds Rob Dekker, Verific's founder and president. "We are delighted to have played a role in this achievement."

Verific's software consists of Verilog, SystemVerilog and VHDL parsers, analyzers and elaborators, and a netlist oriented database. They serve as the front end to the most popular Electronic Design Automation (EDA) tools, including Real Intent's Ascent(TM) for automatic verification, and Meridian CDC(TM) and Meridian FPGA(TM) for Clock Domain Crossing (CDC) for ASIC and FPGA designs. Verific's software is written in platform-independent C++ that compiles on Solaris, HP-UX, Linux and Windows platforms. Each is licensed as source code and come with support and maintenance.

About Real Intent

Real Intent is extending breakthrough formal technology to critical problems encountered by design and verification teams worldwide. Real Intent's products dramatically improve the functional verification efficiency of leading-edge application specific integrated circuit (ASIC), system-on-chip (SoC) and Field Programmable Gate Array (FPGA) devices. Over 40 major electronics design houses worldwide use Real Intent software. Real Intent is headquartered at 505 North Mathilda Avenue, Suite 210, Sunnyvale, CA 94085, phone: (408) 830-0700 fax: (408) 737-1962, web: www.realintent.com, e-mail: info@realintent.com.

About Verific Design Automation

Verific Design Automation, with offices in Alameda, Calif., and Kolkata, India, is a leading provider of SystemVerilog, Verilog and VHDL front-end software founded in 1999 by EDA industry veteran Rob Dekker. Verific's software is used worldwide in synthesis, simulation, formal verification, emulation,



debugging, virtual prototyping, and design-for-test applications, which combined have shipped more than 50,000 copies. Corporate headquarters is located at: 1516 Oak Street, Suite 115, Alameda, Calif. 94501. Telephone: (510) 522-1555. Facsimile number: (510) 522-1553. Email: info@verific.com. Website: www.verific.com.

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