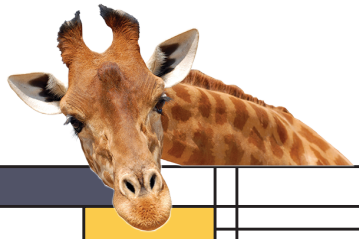


head and shoulders above the rest...

Verific Design Automation

Highlights

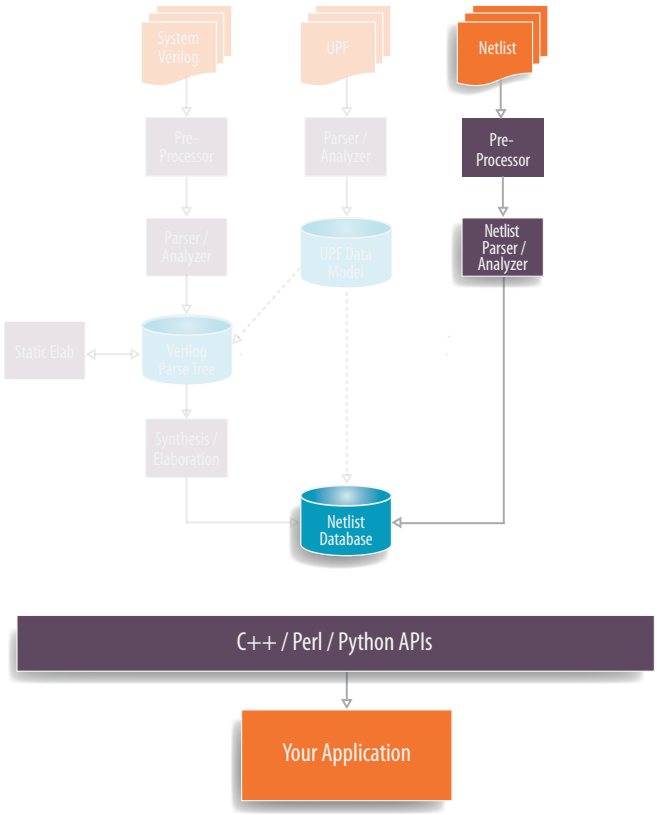
- Parses structural subset of Verilog-2001 (IEEE-1364 standard)
- Support for Verilog and Liberty libraries
- Includes Verific's hierarchical database
- Shipped as C++ source code
- EDIF 2 0 0 included
- Complete line / file origination
- Fully compatible with Verific's RTL parsers / elaborators

VERILOG NETLIST ONLY PARSER

with hierarchical database

Verific's **Verilog Netlist Only Parser** reads a Verilog structural netlist directly into Verific's hierarchical database. It does not create any intermediate parse tree or other persistent data structure.

The Verilog Netlist Only Parser can be of great use to EDA applications that do not (yet) require RTL support. Because no elaboration or parse tree creation is involved, it is aggressively priced. As with all Verific's software, the product is shipped as C++ source code and backed with a rigorous support and maintenance program.



The hierarchical netlist database is identical to the one created by Verific's RTL parsers and elaborators, and allows full manipulation of all objects (ports, wires, cells) such as

- Find, insert, remove, and change
- Keep / flatten hierarchy
- Group / ungroup

Existing attributes on netlists are preserved and vendor-specific attributes can be added at will. Complete line/file information on incoming netlists is maintained and a comprehensive error handler is included.

And, if RTL support becomes required in the future, Verific's (System)Verilog and VHDL parsers bolt straight onto the netlist database.

"Technology that does not differentiate your product from your competitors should be classified as context and outsourced with all possible speed, thereby freeing up time, talent, and management attention to the next wave of core differentiation."

Geoffrey A. Moore, '*Living on the Fault Line*'

Netlist Parser and Database

- Parses > 100,000 netlist lines / second.
- Average memory usage approximately 300 bytes / instance.
- Full hierarchy support, with grouping/ungrouping, etc.
- Find, insert, remove, and change of cells, ports, and wires.
- Full support for any number of libraries, and no restrictions on library interaction (instantiations across different libraries).
- Support for busses.
- Compact storage of line and file origination.
- Simple and clean data model and Procedural Interface.
- Comprehensive error handler.

Support and Maintenance

- On-line, customer accessible defect and enhancement tracking.
- Standard monthly releases with enhancements and improvements.
- 24 hour turnaround for critical defects.

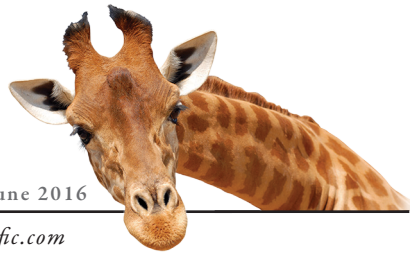
Royalty-free Source Code Licenses

Verific Design Automation ships its software as C+ source code, including makefiles for Unix and Windows platforms. Customers can choose between time-based licenses or perpetual licenses, both of which are always royalty-free. Maintenance and support is included with time-based licenses, and is optional for perpetual licenses.

About Verific Design Automation

Verific Design Automation, with offices in Kolkata, India, and Alameda, CA, was founded in 1999 by EDA industry veteran Rob Dekker. A leading provider of SystemVerilog, UPF, and VHDL front-ends, Verific's software is used worldwide in synthesis, simulation, formal verification, emulation, debugging, virtual prototyping, and design-for-test applications, which combined have shipped over 60,000 copies.

Verific
Design Automation



June 2016