SystemVerilog and the Triangle of Truth

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With the advent of the IEEE 1800-2009 SystemVerilog standard, currently still in the proposal stage but coming up real soon now, we thought it would be a fun exercise to take stock of support for the 1800-2005 version of this mighty hardware description language. For this purpose, we compared the 2 leading SystemVerilog simulators Questa (from Mentor Graphics) and VCS (from Synopsys) with our own Verific SystemVerilog parser, a front end widely used in EDA applications marketed by our customers.

As a besides for those not familiar with Verific Design Automation, we build VHDL, Verilog, and SystemVerilog parsers, analyzers and elaborators, and license those to a wide variety of semiconductor, FPGA, and EDA companies. A representative list of our customers can be found on our website and there is no need to bore the reader with those here. Changes are, if you do RTL design there is a high chance you have used one of our parsers. We never disclose which components our customers' license from us, but we have our fair share of SystemVerilog licensees and carry the battle scars to prove it. We also have a SystemVerilog test suite that we run in-house to validate our own results, and several of our customers have licensed this test suite as well.

Our suite contains 2500 tests with positive tests ('this should pass') and negative tests ('this should fail'). The majority of these are semantics tests, and 40 % is synthesizable. By no means do we claim that this test suite is complete or even sufficient. As a matter of fact, its size dwarfs next to our Verilog 2001 and VHDL regression suites. But, we are sure that over time we will be able to extend our test suite as more SystemVerilog design activity starts occurring in the industry.

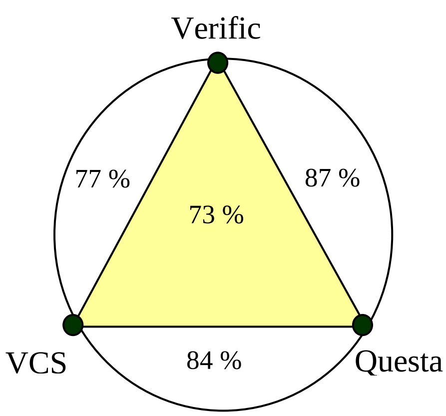
Our experiment was very simple. We took the tests from our SystemVerilog test suite and ran them simultaneously with VCS version 2008.12, Questa version 6.5a, and Verific 2009.01. We aptly named it the 'Triangle of Truth' and categorized the results in 8 bins ranging from '0 0 0' (all 3 tools parse and report the same error on the test) thru '1 1 1' (all 3 tools parse the test). The good news is that in 73 % of the tests all 3 parsers fully agreed. The bad news of course is that that also means there are discrepancies in the remaining 27 %.

The bin where Questa and VCS both successfully parse the test but Verific failed were considered defects and quickly fixed in the Verific parser. There is also a category where both VCS and Questa reported an error in the design as expected but where Verific failed to flag the error. These results are called ‘false positives’ and require improved semantic checking in the Verific parser. They are less onerous but should get fixed over time as well.

And then there were the situations were either Verific and Questa agreed, or Verific and VCS agreed, but not Questa and VCS. Do you remember the saying about the person with 2 watches who never knows what time it is ? Well, that’s how we feel in situations like that. Questa customers of course nudge us towards their simulator’s implementation, and VCS users like it the exact other way. So where does that put us ? Between a rock and a hard place ☺

The worst, of course, is in those situations where one of those leading EDA tools clearly violates the standard. What are the others to do ? Fortunately, that happens only rarely. The conflicts between the three vertices of the ‘Triangle of Truth’ mainly relate to design checking, where tool A issues an error whilst tool B parses the very same design just fine or vice versa.

It will be interesting to see what the 1800-2009 version of the SystemVerilog standard will do to the Triangle of Truth. Improved clarity of the standard should make it easier for the EDA tools to agree on interpretation, but the additions to the language will undoubtedly generate their own category of mismatches. Whatever way it goes, the Triangle of Truth will remain a very useful tool to measure SystemVerilog interoperability.



In our experiment, Verific-VCS-Questa agreed 73% of the time.

VCS-Verific agreed 77 %.
Questa- Verific agreed 87 %.
VCS – Questa agreed 84 %.

First published on EDA Graffiti, www.edn.com, June 17, 2009