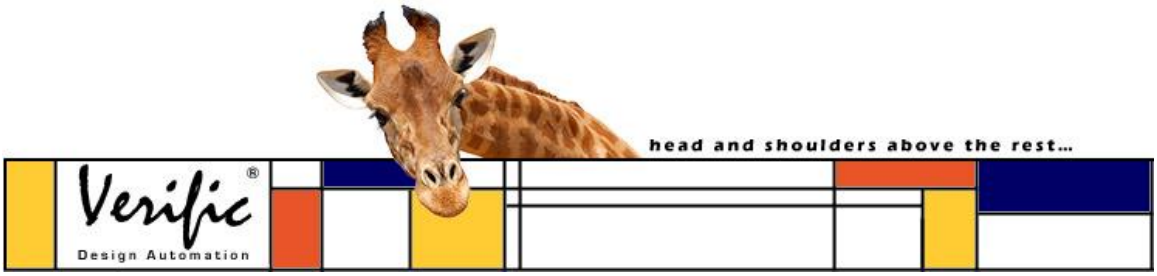

The demise of VHDL has been greatly exaggerated

I don't recall when it was the first time that I heard VHDL was a dying language, but for sure it was many years ago, maybe as far back as the late 1990s. Obviously the EDA futurists of then got it very wrong, and I was recently wondering if I could put a number on how wrong.

At Verific, as the premier provider of SystemVerilog and VHDL parsers to many EDA, FPGA, and semiconductor companies, we do have some good insights in what our customers license from us and how they use it.

Since inception, Verific has shipped just over 100 licenses. So I sat down and tallied the HDL languages these companies obtained from Verific during that period. Here is the countdown

All aggregate licenses over time (includes non-active)

- 97 % licenses Verilog / SV
- 76 % licenses VHDL

All currently active licenses

- 98 % licenses Verilog / SV
- 75 % licenses VHDL

Although not as popular as (System)Verilog, VHDL is clearly holding its own.

We also noticed the continuing interest in VHDL a few years back when many of our customers started inquiring about VHDL-2008 support. Believe me, they wouldn't do that if it wasn't for their end-users requesting it. The answer, would you care, is 'fully supported'. Finally, when some SystemVerilog end-users submitted enhancement requests to support import of VHDL packages in their SystemVerilog designs (no, I am not kidding) we knew VHDL was here to stay.

At Verific, we don't play favorites. As long as the market requests them, we'll keep providing SystemVerilog and VHDL parsers alike.

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