
# The economies of outsourcing

## Verilog and VHDL join the ranks of Context Technology for EDA companies

In his 2000 book 'Living on the Fault Line', high-tech guru Geoffrey Moore (of 'Crossing the Chasm' fame) makes an eloquent case for corporations to focus on *Core* and outsource *Context*. In Moore's view, Core are the activities that directly affects the competitive advantage of an organization, in other words differentiate it from the competition. All other activities, and those are often the bulk of an organization, are Context. The important message, of course, is that one should outsource its Context and focus its best and brightest on its Core. The good news is that one company's Context is another company's Core. An example is the paper multiplication industry. Having a photocopy machine at work is handy, but once a manual needs to be reproduced for customer ship wouldn't you rather go to Kinko's. They pick up and deliver your materials, keep their machines humming 24 hrs a day, and are a lot cheaper than you burning the midnight oil changing your office copier's toner. The time saved should be used on planning your next product.

The Core versus Context discussion is often related to the *Buy* versus *Make* question. If a good solution is available for a well-defined problem, why bother re-inventing the wheel and providing a home-grown solution. Chances are that the task at hand is Context to your application anyhow. And, through purchase, you may very well accelerate introduction of your Core product by many months.

This concept of Core versus Context is applicable to many industries, including Electronic Design Automation (EDA). Most EDA companies have already outsourced some Context activities in their EDA tools, such as License Managers. Why would anyone bother writing their own software for licensing management if the same can be achieved with production proven software from Macrovision (Globetrotter), a third party software company selling FlexLM. It will never make a difference during the evaluation and purchase decision of the EDA tool, the company's Core offering. (The argument can even be taken a step further. Not using the industry standard Licensing Manager may be considered a negative by the customer. After all, now the customer has to learn and manage a new licensing mechanism.)

Hardware Description Language (HDL) front-ends, for long the Core of synthesis companies such as Synopsys, Synplicity, and Exemplar Logic, have entered the ranks of Context for most EDA companies. Nowadays, EDA products in such diverse fields as Design for Test, Formal Verification, Synthesis, and Emulation all require Verilog HDL and VHDL parsers / elaborators.

As many have found out, building HDL parsers and elaborators is not an altogether easy task. Several man years, not counting future debug activity, typically are required to put a reliable system together. And at the end, it will not differentiate the product from the competition because they support the same Hardware Description Languages. In Moore's view, a much preferred solution would be one to acquire a production proven, fully debugged HDL front-end and focus your engineering team on your Core Competency, whether that is in Formal Verification, Emulation, Hardware Acceleration, or Design for Test.

To find out if your HDL front-end is Core or Context and whether outsourcing it may be for you, you can ask yourself the following questions:

- Does it make your company more competitive ?
- Can you distinguish your company from the competition with your HDL front-end ?
- Do you have the expertise in house to build and support it ?
- Are you prepared to support future language extensions ? (Think Verilog 2001, SystemVerilog.)
- Do you want to get your product out to market months earlier ?

Chances are you find out your Verilog and VHDL support are merely Context to your application, necessary but non-discriminating. And that may be the time to start looking around for a solution from a company that makes HDL front-ends its Core.

**About Verific Design Automation**

Verific Design Automation was founded in 1998 by EDA industry veteran Rob Dekker. Prior to founding Verific, Dekker was a software developer, manager, and director at Exemplar Logic. Verific's HDL front-ends are used worldwide in synthesis, formal verification, emulation, debugging, virtual prototyping, and design-for-test applications, which combined have shipped over 20,000 copies.