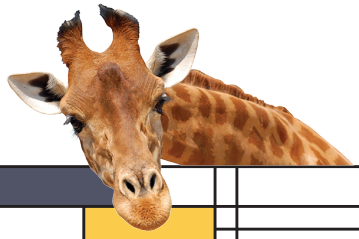


head and shoulders above the rest...

Verific Design Automation

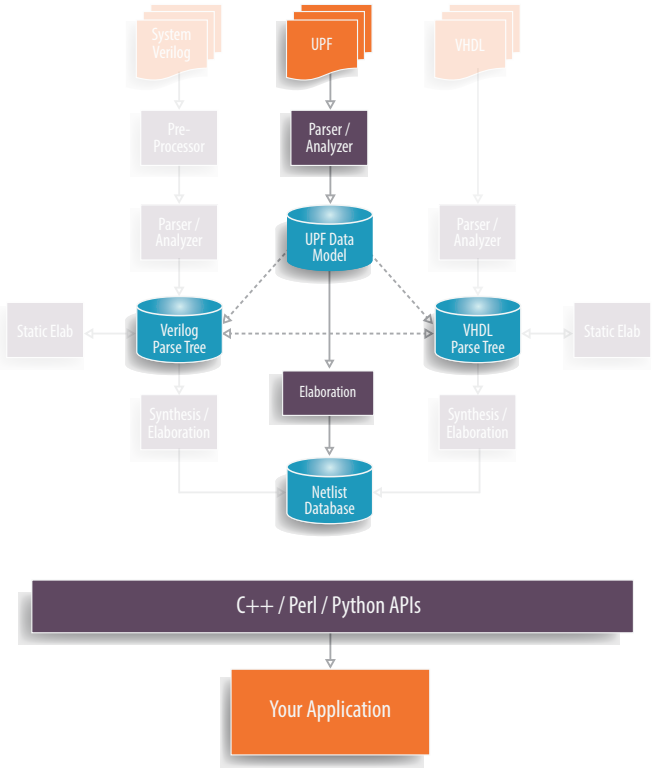
Highlights

- UPF IEEE 1801-2009 / 2013 / 2015 / 2018 parser, analyzer, and elaborator
- Supports UPF 1.0, 2.0, 2.1, 3.0, and 3.1 versions
- Shipped as C++ source code
- Retains file / line /column origination for reporting purposes
- Supports interfacing with external elaborated design data.
- Fully compatible with Verific's SystemVerilog and VHDL parsers

UPF PARSER

The IEEE 1801 Unified Power Format (UPF) standard provides a hardware description language independent way of annotating a design with power intent. UPF allows the partitioning of a design into power domains, resulting in a power intent model containing power management logic and the corresponding supply network needed to power each design element.

Verific's UPF Parser/Analyzer performs syntax and semantic checking, resolving a UPF specification into a power intent model that can then be traversed and queried. The UPF Elaborator applies the power intent model to the original HDL design. The result is a power-aware netlist with new instantiations of power-related cells, as well as any required supply network and corresponding control path logic.



UPF concepts elaborated in an HDL design include logic and supply ports and nets, power switches, and retention, isolation, level-shifter and repeater cells. It is an integral component of Verific's Parser Platform and interacts seamlessly with Verific's standard SystemVerilog, VHDL, and Liberty parsers. It natively interfaces with Verific data structures, and also has the ability to interface with external (non-Verific) design data.

Complete file / line / column information on UPF descriptions is maintained and Verific's comprehensive message handler is included.

"Technology that does not differentiate your product from your competitors should be classified as context and outsourced with all possible speed, thereby freeing up time, talent, and management attention to the next wave of core differentiation."

Geoffrey A. Moore, '*Living on the Fault Line*'

UPF Parser

- Compact storage of file, line, and column origination.
- Simple and clean data model and procedural interface.
- Comprehensive error handler.
- Interfaces with Verific's native data structures.
- Supports interfacing with external, non-Verific data structures.
- Elaborates power intent into netlists (logic / supply ports and nets, power switches, and retention / level-shifter / repeater cells).

Support and Maintenance

- On-line, customer accessible defect and enhancement tracking.
- Standard monthly releases with enhancements and improvements.
- 24 hour turnaround for critical defects.

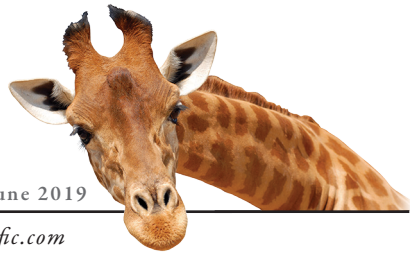
Royalty-free Source Code Licenses

Verific Design Automation ships its software as C+ source code, including makefiles for Linux, Mac, and Windows platforms. APIs are available in C++, Perl, and Python. Our time-based licenses are royalty-free and include maintenance and support.

About Verific Design Automation

Verific Design Automation, with offices in Kolkata, India, and Alameda, CA, was founded in 1999 by EDA industry veteran Rob Dekker. Prior to founding Verific, Dekker was a software developer, manager, and director at Exemplar Logic. The defacto standard for SystemVerilog and VHDL front-ends, Verific's software is used worldwide in synthesis, simulation, formal verification, emulation, debugging, virtual prototyping, and design-for-test applications, which combined have shipped over 60,000 copies.

Verific
Design Automation



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