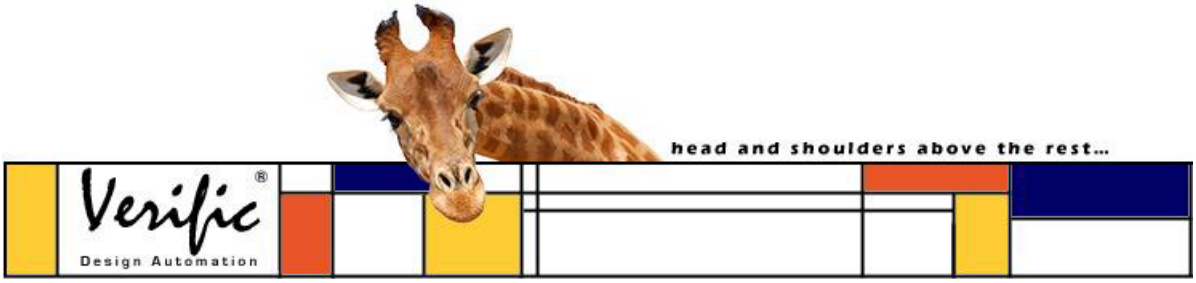

CASE STUDY:
Verific and Vorak Solutions Bring State-of-the-Art Features and Performance to Rapid Silicon's FPGA Design Suite

In this case study, we learn how Verific Design Automation's HDL parser platform was used by the consulting team at Vorak Solutions to create a new synthesis flow for Rapid Silicon's FPGA design suite. This collaboration brought together the expertise of all three teams to create a high-performance synthesis tool with 2X better performance versus other competitors when using the EPFL benchmark suite.

Overview

Todays' digital logic designs are described in Hardware Description Languages (HDL) that are fed to synthesis tools to create gate-level logic, which is then fed to a place-and-route (PNR) tool to create a layout. For field programmable gate-array (FPGA) hardware, a bitstream is generated to program the logic elements on the chip to implement the final design.

Verific's industry standard platform is used for reading HDLs – SystemVerilog, Verilog and VHDL designs and functional digital blocks (IP) – into design environments. One reason for its leadership is Verific's full support for all of the various VHDL, Verilog, and SystemVerilog standards. This means that the parsing and elaboration of the digital logic described in the HDLs is done quickly, with a minimal resource footprint, and that a full feature set of operators for manipulating and traversing the logic design across hierarchies and levels is provided.

Verific's business model has the flexibility to support new startups such as Rapid Silicon that provide synthesis, simulation, and hardware implementation software.

Turning to the end-user of Verific's parser platform, Rapid Silicon, we will show how it was deployed in their Raptor FPGA electronic design automation (EDA) environment. Raptor is the world's first commercial tool chain using open-source software from beginning-to-end. The open-source nature of Raptor means that the entire design community and ecosystem collaborate to make it the best in the business. See Fig. 1 for an illustration of the tool-set in the Raptor environment.

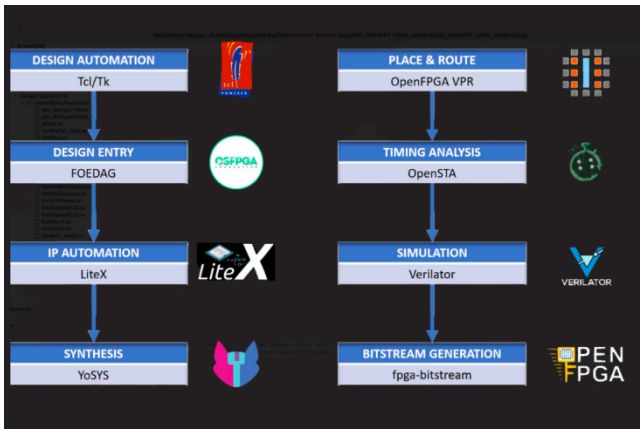

Fig. 1. Tool names and providers' logos for the open-source software suites used in the Raptor FPGA design environment of Rapid Silicon. (Source: Rapid Silicon)

The remainder of this case study focuses mainly on the Raptor synthesis tool, YoSYS, which was extended and developed to meet the requirements of Rapid Silicon and its customers.

Extending YoSYS

The open-source community for digital design software has many projects and efforts to assist hobbyists, and researchers in creating new hardware designs at minimal cost. By lowering the cost of EDA software, the bar to entry for new projects and designers is much lower. This accelerates the quality and quantity of solutions that can be produced. In addition, efforts from university researchers, and industry innovators, continue to advance the feature set and performance of the EDA project software to deliver a world-class offering.

So it is no surprise that Rapid Silicon adopted the synthesis tool YoSYS that has been under development for over 10 years. It should also be noted that Verific already had an existing relationship with the YoSYS development team at YoSYSHQ. They had implemented hooks to Verific's front ends so YoSYS could reliably import Verilog 2005, SystemVerilog and VHDL designs. As a result, end-users can purchase from YoSYSHQ a fully supported, Verific-enabled version of YoSYS called TabbyCAD.

Rapid Silicon's goals for commercializing Raptor included providing the same level of HDL coverage as was available in mainstream FPGA offerings, which, not surprisingly, are all equipped with Verific's front-ends. This meant supporting the IEEE-1800 standard (2017, 2012, 2009, 2005) for Verilog/SystemVerilog, and the IEEE-1076 standard (2008, 1993, 1987) for VHDL. This complete capability also supported a mix of both languages. This is especially important for using established IP blocks that may be in either of the two languages.

Besides wanting to provide the best FPGA synthesis performance based on industry standard benchmarks, a further goal for Rapid Silicon was to extend both the Random Access Memory (RAM) and Digital Signal Processor (DSP) inference capabilities of YoSYS. The base capability of YoSYS was to be extended from several inference types to more than 40. To create this large number of inferences from

an HDL for RAMs and DSPs requires extensive programming and hardware expertise. This was when Vorak Solutions began their work with Rapid Silicon.

Vorak's engineering expertise and knowledge of the Verific parser platform has been used to develop numerous applications and programs for several Verific customers including Rapid Silicon and other noted semiconductor companies.

Vorak accelerates application development projects for customized solutions, product development and testing. In one example, a floorplan estimator was developed for a Verific customer who needed block-level initial estimates. In another, Vorak designed a custom hierarchy report that specified characteristics at each level of the design hierarchy.

Alain Dargelas, VP of Software Engineering at Rapid Silicon, said about Vorak Solutions: "We knew that the core of the Vorak team provided services for another FPGA startup, Tabula. Vorak has theengineering skills and experience, for digital synthesis development including parsing, and front-end tool development. Their offshore team reduces costs by 50% compared to domestic software development, without any compromise reflecting the quality of the Armenian team. And the team is very stable. They know their stuff."

Georgi Mikichyan, COO at Vorak, described the connection with Verific: "We have a close collaboration with Verific, and are a trusted partner. With access to the same source code, we can fix issues and deliver them to Verific. Our regular discussions with their team go hand-in-hand with their excellent support. We are happy to provide added value to Verific."

In Fig. 2, we see a summary of the major extensions that were made to the YoSYS synthesis tool in the Raptor flow.

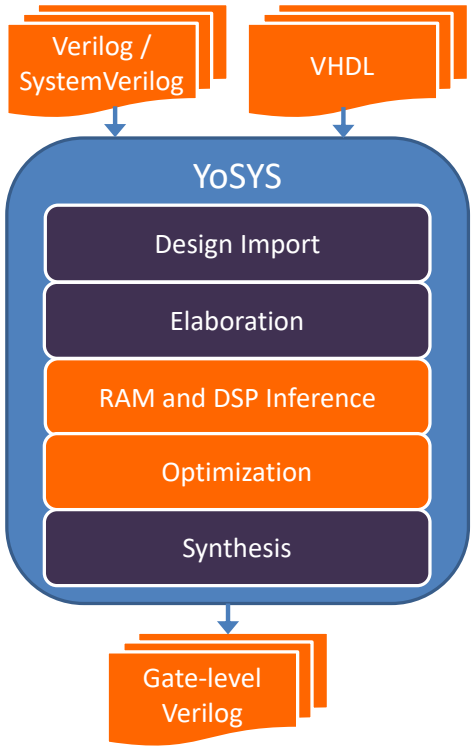

Fig. 2. Improvements to the YoSYS synthesis tool shown in orange. (Source: Rapid Silicon)

Leading Edge Synthesis Performance

In 2022, Rapid Silicon's Raptor was awarded 24 verified unique wins and two ties, double the number of wins versus the leading competitor, in the latest École polytechnique fédérale de Lausanne (EPFL) Combinational Benchmark Suite for best Boolean optimization performance. This strong showing in the EPFL competition is attributed in large part to Rapid Silicon's patent-pending "ABC-DE" algorithm.

The EPFL Combinational Benchmark Suite is an open competition to test the efficiency of synthesis, in both implementation size and performance. It is used to define new comparative standards for the logic optimization and synthesis community. The latest open-source benchmark suite includes approximately 20 combinational designs comprised of 10 arithmetic computational algorithms and 10 random and control designs, which are intentionally not optimized in order to test the ability of synthesis and optimization design tools. These sub-optimal designs are then synthesized to a LUT-6 architecture. The EPFL results are verified by an independent committee then published as confirmed winners. The latest competition results can be found on the EPFL website[1].

Other Raptor Improvements

[1] See https://github.com/lsils/benchmarks/tree/master/best_results

The Verific parser platform has also been used by Rapid Silicon to further develop the commercial capabilities of the Versatile Placer and Router VPR tool from the OpenFPGA project, which is used after YoSYS synthesis.

VPR was enhanced to use Verific's gate-level Verilog parser to read and write, encrypted gate-level Verilog in support of an encrypted hardware design chain. This provided a secure framework for sharing routed digital designs with partners and clients.

In addition to VPR enhancements, Vorak was instrumental in developing a plug-in system for a specific FPGA architecture, technology mapping to a foundry technology process node, and porting Raptor to the Microsoft Windows operating system.

Georgi Mikichyan, at Vorak, described their work with other clients when deploying the Verific parser platform, "We are very familiar with the Verific software interfaces, and we can quick-start projects easily. In one case, a floorplan estimator was developed for a Verific customer who needed block-level initial size estimates. We have also designed a custom hierarchy report that aggregated some characteristics at each level and elaborated others. Each designer got a detailed view of their part of the design while retaining a global analysis. In summary, we know FPGA and ASIC design flows, and can provide glue logic and integration of components to EDA companies."

Vorak was an integral part of the development team for Raptor and contributed to its enhancement including quality assurance (QA), validation, quality of results (QoR) profiling and benchmarking. The Vorak team was fully integrated into the Rapid Silicon design and development systems, including code reviews and measuring test coverage. This included code coverage analysis, custom testbench preparation, and formal analysis of RTL versus gate-level logic. Specifically, Vorak integrated Verific's parser platforms with YoSYS synthesis, and optimized the synthesis capabilities at the gate-level and to ensure QoR with respect to the EPFL benchmarks.

Summary

In this case study, we learned how Verific Design Automation's HDL parser platform was used by the consulting team at Vorak Solutions to create a new synthesis flow for Rapid Silicon's FPGA design suite, Raptor. This collaboration brought together the expertise of all three teams to create a high-performance synthesis tool set with 2X better performance versus other competitors when using the EPFL benchmark suite. As well, synthesis and inference capabilities were enhanced for RAM and DSP design blocks, and the Raptor suite was ported to the Windows operating system. This was achieved by Vorak's team on-time with high quality at significantly lower cost.

Vorak Solutions expertise and focus on quality in both coding and synthesis results met the reliability and QoR needs of Rapid Silicon, which in turn made Rapid Silicon customers successful and satisfied with their FPGA designs.

Verific's flexible business model and full support of industry standard HDLs in its parser platform enables new commercial startups such as Rapid Silicon to meet their requirements to support sophisticated and world-class hardware design.

About Rapid Silicon

Rapid Silicon is a provider of AI and intelligent edge-focused FPGAs based on open-source technology. The company's products are designed to meet the needs of AI and intelligent edge developers and help them accelerate their time-to-market. Rapid Silicon's mission is to democratize access to FPGA technology and make it more accessible to developers around the world.

About Vorak Solutions

Vorak Solutions, founded in 2015 in the United States and Armenia, was formed by experienced professionals from both countries based on a long-standing successful collaboration of the management and engineering teams. Vorak, Armenian for Quality, provides high-quality development and quality assurance services in the areas of software, cloud and EDA products at a fraction of first world engineering costs.

About Verific Design Automation

Verific Design Automation is the leading provider of SystemVerilog, Verilog, VHDL and UPF Parser Platforms that enable project groups to develop advanced electronic design automation (EDA) products quickly and cost effective worldwide. With offices in Alameda, Calif., and Kolkata, India, Verific has shipped more than 60,000 copies of its software used worldwide by the EDA and semiconductor industry since it was founded in 1999.