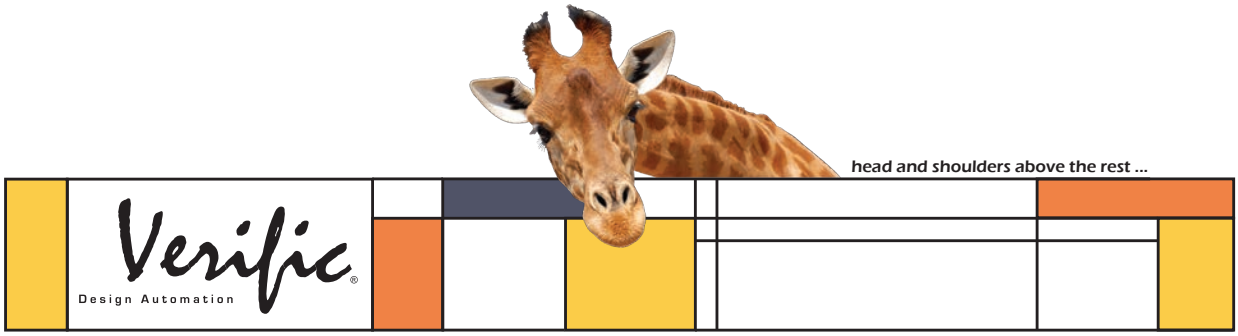


Verific's Parser Platform

- SystemVerilog IEEE 1800-2005 / 2009 / 2012 / 2017 / 2023 parser, analyzer, and elaborators
- VHDL IEEE 1076-1993 / 2002 / 2008 / 2019 parser, analyzer, and elaborators
- UPF IEEE 1801-2009 / 2013 / 2015 / 2018 / 2024 parser. analyzer, and elaborator
- Full mixed SystemVerilog / VHDL language support
- Verilog-AMS 2.4 / VAMS 2023 parser and analyzer
- Hierarchical, technology independent database
- Verilog 2001, SystemVerilog test suites
- C++, Python, and Perl APIs

"It would have been very difficult to achieve our language coverage and quality goals in Vivado without the help of the Verific parsers and elaborators."

Dan Gibbons, Vice President,
FPGA Software Development,
Xilinx

"Verific has become the industry standard and for good reason. The software is first rate and the support is outstanding."

Luc Burgun, CEO, EVE
(acquired by Synopsys)

"We have never worked with a vendor that was so responsive to all our needs and delivered so promptly with such high quality."

Leon Stok, Vice President,
Electronic Design Automation,
IBM

Verific Design Automation **builds SystemVerilog, UPF and VHDL Parser Platforms which enable its customers to develop advanced *EDA products* quickly and at low cost.**

Verific's Parser Platforms **are distributed as C++ *source code* and compile on all 32 and 64 bit Linux, Mac, and Windows operating systems.**

Verific's Parser Platforms **are in production and development use today at numerous companies worldwide, from EDA start-ups to established Fortune 500 semiconductor vendors. Applications vary from formal verification to synthesis, simulation, emulation, virtual prototyping, in-circuit debug, and design-for-test.**

Benefits of Verific's Parser Platforms

Time to Market

- At least 24 month head start with production proven RTL technology.
- No need to recruit and staff your own HDL software team.
- No need for extensive test and debug of your HDL solution.
- Immediate acceptance of RTL front end by semiconductor industry.

Focus

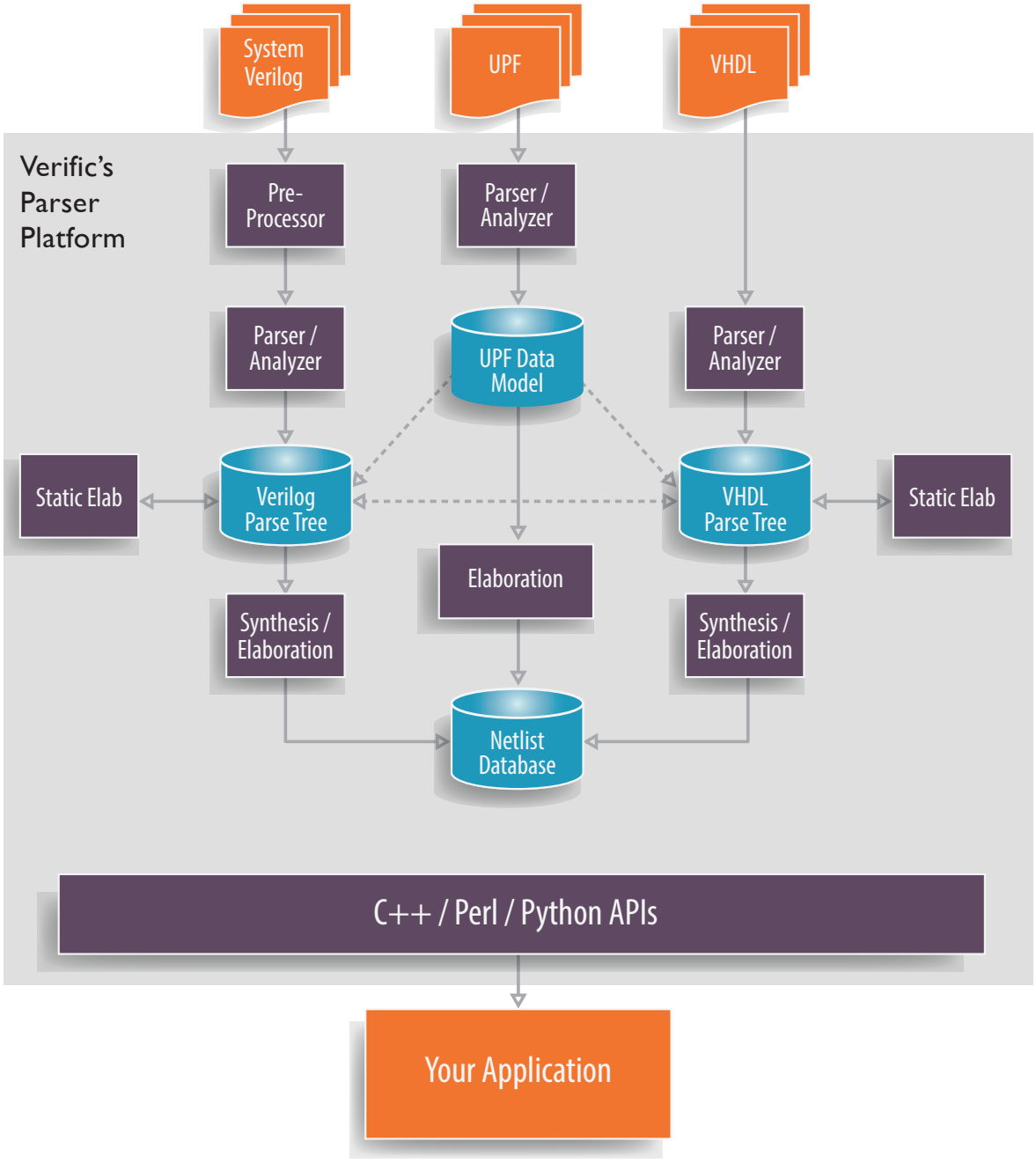
- Concentrate on the strategic, differentiated core of your application.
- Don't waste time and talent on non-strategic HDL software.

Quality

- Prevent lost sales due to an immature HDL front-end.
- Prevent high support costs due to bugfix releases and workarounds.

License Models

- Our licenses are always royalty-free. We ship Source Code to our customers, allowing you full control over modifications, extensions, integration, and compilation.
- Our time-based licenses have no upfront cost, can be cancelled anytime, and include maintenance and support.
- If there is a technical match, we will find a license arrangement that fits your needs.



"Verific's SystemVerilog solution was referred to us by one of our key strategic accounts. Our assertion technology requires extensive language elaboration, all of which Verific fully supports."

Yunshan Zhu, CEO,
Nextscope (acquired by Synopsys)

"Quartus II, Altera's flagship design software includes integrated VHDL and SystemVerilog technology from Verific. Verific's software meets the high standard of quality our customers have come to expect from us."

Premal Buch, VP Software
Engineering, Altera

Verific®
Design Automation

Verific Design Automation, Alameda, CA (510) 522-1555 www.verific.com

Verific's software is integrated in a variety of EDA products, including:

Achronix	ACE
Aldec	ALint, HES
Altair	RTLVision Pro
Altera	Quartus II
Arteris	IP-Xact platform
Ansys	PowerArtist
AMD	internal use
Arcas	Avista
Ausdia	TimeVision
Baum	PowerBaum
Blue Pearl	Analyze RTL
Cadence	CellMath, JasperGold, RocketSim
Cycuity	Prospect
DeFacTo	STAR-RTL
Efinix	IDE
Empyrean	Clock Explorer, Alps
Excellicon	ConMan
Fudan	Procise
Gowin	Gowin EDA
Google	internal use
HDL Works	HDL Companion
IBM	Morph
Infineon	Inway
Innergy	Power Analysis
iRoC	SoCFIT
Lattice Semi	ispLever
Mediatek	internal use
Menta	Origami
Microsemi	Libero
NanoXplore	NanoXmap
NEC	CyberWorkBench
Nvidia	internal use
NXP	internal use
Qualcomm	Qbreeze
Real Intent	Ascent, Meridian
Renesas	internal use
S2C	Prodigy
Samsung	internal use
Siemens EDA	RealTime Designer, Annealer, Clarus, SLEC, Powerpro, Crossfire
Socionext	internal use
STMicro	internal use
Synopsys	FineSim
Tiempo	ACC
VSync	vChecker
YosysHQ	Tabby CAD
Xilinx	Vivado

"Verific's language solutions, combined with Jasper's assertion synthesis technology, have contributed to our leading position in formal verification."
Claudionor Coelho, VP engineering,
Jasper (acquired by Cadence)

Verific is a Platform

"Technology that does not differentiate your product from your competitors should be classified as context and outsourced with all possible speed, thereby freeing up time, talent, and management attention to the next wave of core differentiation."

Geoffrey A. Moore,
Living on the Fault Line

Production Proven SystemVerilog and VHDL Platforms

More than 60 EDA, FPGA and semiconductor companies are shipping products incorporating Verific's SystemVerilog and VHDL front-ends, with a combined customer base of more than 60,000 users. Instead of writing your own, you can buy and incorporate our C++ source code, fully tested and production proven. And, because Verific ships Source Code, you still retain full control over all modifications, extensions and integration.

Royalty-free, Time-based Source Code Licenses

Verific Design Automation ships its software as C++ source code, including makefiles for Linux, Mac, and Windows platforms. Our time-based licenses are royalty-free and include maintenance and support.

Choose your platform: C++, Python or Perl

Verific's parsers, analyzers, and elaborators are all written in C++. Its APIs are available in C++ as well as Python and Perl.

"We replaced our existing Verilog and VHDL parsers and elaborators with Verific's solution."
Tomat Miller, VP engineering,
Apache (acquired by Ansys)

"Integrating Verific's software with RealTime Designer had been a part of our product planning and development from the beginning because of its superior quality."
Paul van Besouw, CEO,
Oasys (acquired by Mentor)

"We have employed Verific's SystemVerilog parser for several years within our internally developed EDA tools."
Dan Smith, senior director,
hardware engineering, NVIDIA

"Verific and Calypto have been development partners for many years. Verific's team is exceptional and its support is unmatched."
Nikhil Sharma, VP engineering,
Calypto (acquired by Mentor)

Verific®
Design Automation

VHDL Platform

- Parses, analyses and elaborates 50,000 lines/second RTL or more.
- 100% VHDL IEEE 1076-1993/2002/2008/2019 language coverage.
- Auto discovery and file sort, -F file list support.
- Includes synthesis subset checking.
- Best in class support for elaboration, including IEEE 1164, multiple libraries, records, multi-dimensional arrays, generics, configurations, user-defined and overloaded functions/procedures/types, variable-indexing etc.
- Support for all standard and de-facto standard synthesis packages.
- Support for all Cadence, Siemens EDA, and Synopsys synthesis pragmas.
- Downstream error handling support with line/file origination storage in RTL database.
- Application specific compile and run-time switches (don't care info, object preservation, etc.).

SystemVerilog / Verilog Platform

- Parses, analyses and elaborates 60,000 lines/second RTL or more.
- 100% SystemVerilog IEEE 1800-2005/2009/2012/2017/2023, including Verilog IEEE 1364-1995/2001/2005 language coverage.
- Auto discovery and file sort, -F file list support.
- Includes synthesis subset checking.
- Built-in Verilog pre-processor.
- Best in class support for elaboration, including memory, named ports, tasks, functions, variable-indexing, string constants, etc.
- Verilog XL compliance with unknown module instantiation, and -y/-v file search mechanisms.
- Support for all Cadence, Siemens EDA, and Synopsys synthesis pragmas.
- Downstream error handling support with line/file origination storage in RTL database.
- Application specific compile and run-time switches (don't care info, object preservation, etc.).

UPF Platform

- 100% UPF IEEE 1801-2009 / 2013 / 2015 / 2018 / 2024 language coverage.
- Fully integrated with Verific's SystemVerilog and VHDL platforms.
- Stores file / line / column origination for reporting purposes.
- UPF Elaboration resulting in a power aware netlist

RTL Database

- Average memory usage approximately 600 bytes / instance.
- Full hierarchy support, with grouping/ungrouping, etc..
- Compact storage of line, file and column origination info from RTL parsers.
- Simple and clean data model with procedural interface for easy integration with your existing database.

About Verific Design Automation

Verific Design Automation, with offices in Kolkata, India, and Alameda, CA, was founded in 1999 by EDA industry veteran Rob Dekker. The defacto standard for SystemVerilog, UPF and VHDL parsers, Verific's software is used worldwide in synthesis, formal verification, emulation, debugging, virtual prototyping, and design-for-test applications, which combined have shipped over 100,000 copies.

Verific® Design Automation

June 2024