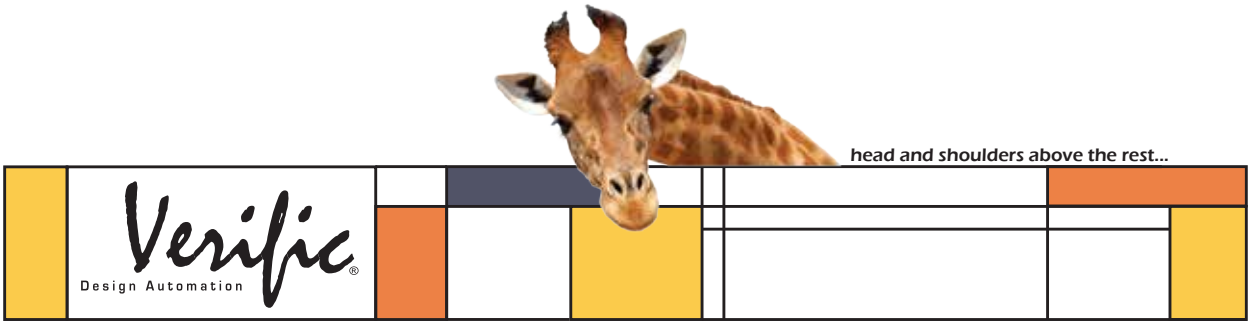


# THE VERIFIC EDA STORE

Verific's SystemVerilog, VHDL, and UPF Parser Platforms have been the foundation under EDA tools and flows at companies worldwide. Now a toolkit with example applications that showcase a variety of point tools and solutions built with Verific's Parser Platforms are available in the Verific EDA Store.

Currently available in the Verific EDA Store are:

## LintRTL

A Linter tool for SystemVerilog and VHDL. Identify design issues early with configurable lint rules and advanced synthesizability checks.

## SnapRTL

An automated HDL editor. Analyze, modify, and export designs while preserving your original code and formatting. Modify with confidence!

## TraceRTL

A Signal Tracer for SystemVerilog and VHDL. Improve traceability and speed up debug.

## HierRTL

A Hierarchy Explorer to report the structural hierarchy of Verilog, SystemVerilog, and VHDL designs directly from the parse tree — no elaboration required.

We are actively working on new applications that will be added over time.

## You can download the tools in the Verific EDA Store at

# STORE.VERIFIC.COM

You don't need to be an existing Verific customer, but we require you to register. New users will be asked to register with a Verific Passport account. Once you have an account you can sign in and will be taken to the product page. Basic tools are currently free, but advanced features require a monthly subscription fee.

Free of charge evaluations are available for 14 days.

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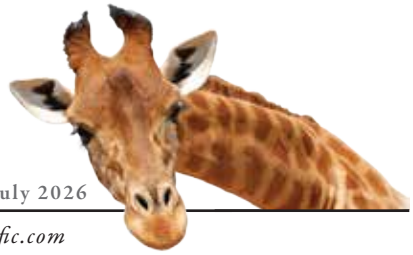
## About Verific Design Automation

Verific Design Automation, with offices in Kolkata, India, and Alameda, CA, was founded in 1999. A leading provider of SystemVerilog, VHDL, and UPF front-ends, Verific's software is used worldwide in synthesis, formal verification, emulation, debugging, virtual prototyping, low power design, and design-for-test applications.

Verific
Design Automation



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